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(54) **Memory requirement reduction in a SQTV processor by ADCPM compression**

(57) An SQTV processor for converting a video signal received at an interlaced scanning frequency of 50 or 60 Hz, respectively to an interlaced scanning frequency of 100 or 120 Hz and implementing algorithms of noise filtering and of edge definition, including an analog-digital converter (ADC) of analog input signals of luminance and chrominance, at least a field memory (FIELD MEMORY_1) or more preferably two similar field memories where digital blocks of luminance (Y) value and blocks of values of each one of the two chrominance (U, V) components of said converted video signals are stored, one "First-In-First-Out" (LINE MEMORY) register for digital values read from said filed memory containing the pixels of a whole line of each field, a noise filtering block (NOISE REDUCTION), a sampling frequency converter (SRC) of said fields from 50 or 60 Hz to 100 or 120 Hz, means of conversion of the vertical format (VFC), means of edge definition (PE) enhancement and means of digital-to-analog conversion (DAC) of the processed luminance and chrominance (YUV) signals, is further equipped with means for compressing and coding said converted video signals according to an adaptive differential pulse code modulation (ADPCM) scheme of said digital values to be stored in said field memory (FIELD MEMORY_1) and means of ADPCM decoding and decompressing of data read from said field memory (FIELD MEMORY_1).

The significative reduction of the total memory requisite produced by the ADPCM pre-compression would make the entire system more readily integratable on a single chip.

FIGURE 3
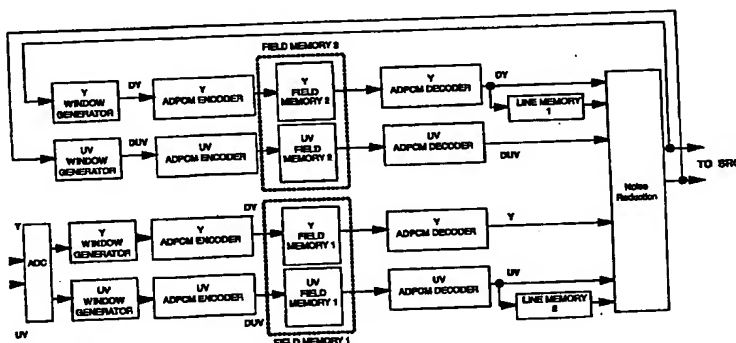
EP 0 797 353 A1

Description

The present invention relates to digital processing systems for video signals received to display images on a TV screen and more in particular to an integrated system, generally known as "Improved Quality Television processor "(IQTV) or "Smart Quality Television processor" (SQTV), requiring storing of whole pictures or parts of them in the decoding phase.

These integrated systems are evermore largely employed in video receivers to improve image quality without requiring changes in the relevant transmission standards (PAL, NTSC, SECAM).

In practice, luminance (Y) and chrominance-U and chrominance-V (UV) analog components of the video signal are digitized through relevant analog-to-digital converters and the digital data obtained, concerning the two fields into which the video signal is generally divided, are stored in a dedicated memory. This allows, first, a conversion from 50 or 60 Hz to 100 or 120 Hz of the interlaced scanning frequency (in practice the so-called "refresh-rate") so to make flickering imperceptible.

Moreover, digital values relevant to each pixel of each line forming each field so stored in the memory, enable to implement appropriate algorithms for reducing gaussian and spike or pulse noise and, through memory duplication, it is possible to implement also a compensation (elimination) loop of blurring of objects moving fast on a background, employing an algorithm that contemplates the calculation of average values among the values of pixels relating to successive pictures, so to eliminate non correlated contents of the video signal and correction algorithms based on motion detection.

In general, the field memory or memories are DRAM devices which according to the present limits of manufacturing technologies, are external to the integrated device containing the processing circuits (generally called SQTV_IC or IQTV_IC).

A common video receiver includes a tuning section, that selects the channel and the relevant frequency band of the signal transmitted via cable, satellite, or terrestrial ether. The tuner converts the received signal to an intermediate video frequency (for example 38.9 Mhz according to the Italian standard) containing luminance and chrominance data multiplexed in frequency. A demodulation block processes the signal converted at intermediate frequency, producing a basic band composite video signal, which is selected by a selector of the input signal source and feeds the standard decoder (PAL, NTSC, SECAM) carrying out the separation of luminance and chrominance components.

Analog signals relevant to luminance (Y) and chrominance (UV) are thus converted through appropriate analog-to-digital converters so to produce a luminance (Y) digital data stream and a chrominance (UV) digital data stream which are fed to the IQTV_IC (or SQTV-IC) device).

Each FIELD MEMORY may store a picture field in the 4:2:2 format or in the 4:1:1 format, thus occupying the following memory space

PAL	720x288x8 for luma (luminance)(Y)	1,658,880 bits	=3,317,760 bits
	360x288x8 for U chroma (chrominance U)	829,440 bits	
	360x288x8 for chroma (chrominance V)	829,440 bits	
NTSC	720x240x8 for luma (luminance)(Y)	1,382,400 bits	=2,764,800 bits
	360x240x8 for U chroma (chrominance U)	691,200 bits	
	360x240x8 for chroma (chrominance V)	691,200 bits	

In the case of a PAL transmission system which, being the more critical standard, can be taken as reference example, the total requisite, when employing two field memories becomes 3,317,760*2 = 6,635,520 bits.

There is the need or usefulness to reduce this memory requisite of a SQTV_IC (or IQTV_IC) without causing a perceivable visual deterioration of images. This in order to save costs and/or create more suitable premises for the integration of the field memory in the same IQTV_IC (or SQTV_IC) chip, through a perfection of manufacturing processes.

The system of the invention is based on compressing and coding according to an adaptive differential pulse code modulation scheme (ADPCM) the digital data relevant to a field in a 4:2:2 or in a 4:1:1 format of a picture to be stored in the relevant field memory at a 50 or 60 Hz standard frequency and on ADPCM decoding and decompressing the data read from the field memory at a multiple frequency (generally double) of the frequency at which the data are written in the field memory.

The ADPCM compression mechanism takes advantage of the correlation existing between adjacent pixel values of a picture to reduce the number of bits required for a binary representation of the picture itself. In fact, it is possible to approximate the pixel values, by suitably combining only the value of pixels adjacent thereto (therefore, not using (stor-

ing) the actual pixel value), that is by implementing a so-called "prediction" of the pixel itself.

Therefore it is possible to reduce the quantity of binary figures required for the digital representation of a picture by defining the prediction mechanism and therefore duly coding (and storing) the prediction error only instead of each pixel. The more accurate is the prediction of the pixel value, the lower is the entropy of the prediction error, or the lower is the number of bits required to code it.

The method of the invention enables in practice to cut down to less than a half the RAM memory requisite for the storing of the field or fields used, with an almost neglectable loss in the quality of reconstructed images because artifacts are mainly distributed at high frequencies.

The various aspects and advantages of the invention will be even more evident through the following description of some important embodiments and referring to the attached drawings, wherein:

Figure 1 is a block diagram of a video receiver including a digitized picture processing system;

Figure 2 shows an example of the architecture of the circuitry for the analog-to-digital conversion, digital processing and digital-to-analog reconversion of Y U V components of the video images;

Figure 3 is a partial diagram showing the architecture modified according to the present invention;

Figure 4 is a diagram of a Window Generator block of the diagram in Fig. 3;

Figure 5 is a diagram showing the ordering in the scanning of pixels of each block for a work windows defined by four lines;

Figure 6 is a diagram showing the scanning of data per blocks in a work window defined by four lines;

Figure 7 is a diagram of the ADPCM coding and compressing block;

Figure 8 is a diagram of the ADPCM decoding and decompressing block;

Figures 9, 10 and 11 show a detailed diagram of the variance evaluation block of the functional diagram of Fig. 7.

Fig. 1 shows a typical functional block diagram of a video receiver.

The tuner (TUNER) selects the channel and the relevant frequency band (for instance RAI2 471 Mhz) and produces a signal converted at a video intermediate frequency (for instance at 38.9MHz according to the Italian standard) containing the luminance and chrominance signals, multiplexed in frequency.

The demodulating block (DEMODULATOR) processes the tuner signal converted at intermediate frequency and produces a base band composite video signal at its output.

Through an input selector (INPUT SEL), the source of video signal (for instance coming from the antenna or cable or from a SCART socket) is selected.

The decoder (STANDARD DECODER) separates the luminance and chrominance components of the composite video signal according to the particular transmission standard (PAL, NTS or SECAM) and sends them to the relevant analog-to-digital converters, represented as a whole in the diagram by the ADC block. Analog-to-digital converters produce a digital stream of luminance (Y) values and a digital stream of chrominance-U and chrominance-V (UV) values which are fed to the SQTV_IC processor which, according to the example considered, dialogues with the two field memories (FIELD MEMORY_1 and FIELD MEMORY_2).

The SQTV_IC processor can be programmed in order to manage data, alternatively formatted in a 4:1:1 or in a 4:2:2 format.

After processing, luminance (Y) and chrominance (UV) components are reconverted by the relative digital-to-analog converters and fed to the inputs of the VIDEO PROCESSOR block for generating deflection signals (RGB).

The chip SQTV_IC may be for instance the PQFP100 device described in the preliminary datasheet (December 1995 edition) of SGS-THOMSON MICROELECTRONICS, whose content is included herein by express reference.

The two field memories FIELD MEMORY_1 and FIELD MEMORY_2 may be implemented in an external DRAM device or integrated in the SQTV_IC chip.

The function performed by the FIELD MEMORY_1 consists in storing a video field every 20ms (in the case of 50 Hz PAL standard). This implies that the next field replaces the previous one after 20ms. Field doubling is obtained by reading the content of the FIELD MEMORY_1 every 10ms.

Therefore in the first 10ms after a field storing, the field is completely read in a "raster" format. In the successive 10ms, prior to storing of a new field, the previous field is read for a second time in "raster" format.

This method of operation can be implemented by employing a random access memory (commonly a DRAM) or a

sequential access memory (generally called FIFO) where the first datum stored is the first to be read and so forth for all data after the first one.

Practically, the FIELD MEMORY_2 is used as a field delay, to enable fields interpolations aiming at eliminating pulse and gaussian noise.

The whole functional diagram of the processing section included in the SQTV_IC is shown more in detail in Fig. 2.

According to a well known architecture, such as that shown in Fig. 2, data relevant to the Y (luminance) and UV (chrominance U and chrominance V) components are written in the field memory FIELD MEMORY_1 in a pre-set format (4:1:1 or 4:2:2) at a writing frequency of 50 (or 60), or 50 or 60 Hz and are read at double that frequency.

The LINE MEMORY_1 block is a buffer, of the so-called "First-In-First-Out" type, capable of delaying each pel (short for pixel) of a scan line of the video picture by a time equal to the "transit" time of a whole line of pixel. This allows to feed pairs of pixels belonging to successive scanning lines and occupying the same position in the line scan (that is they are adjacent to each other in an orthogonal direction to the scan lines) to the relevant inputs of the NOISE REDUCTION block.

In the example considered, a second field memory is also present, FIELD MEMORY_2, to allow implementation of filtering algorithms of non correlated information between two successive image fields so to eliminate (filter) the (non gaussian) pulse noise, according to techniques that are well known to a skilled practitioner.

In practice, correction algorithms for the elimination of undesired or noisy effects of different origin and type can be implemented in the block generally called NOISE REDUCTION. This is possible by virtue of the digitization of the video signal components and their storing at the standard (50 or 60 Hz) transmission frequency and therefore of the possibility to read data stored at a multiple frequency and perform processings suitable to compensate and eliminate undesired effects of different nature and source, as they occur, depending on the video input signal source.

Briefly, an SQTV processor includes a sampling frequency of pictures converter SRC (Sampling Rate Converter), compressing/coding networks as represented in the diagram by the two VFC (Vertical Format Converter) blocks and by the PE (Picture Enhancement) block to emphasize edge definition of pictures, preceded by a "First-In-First-Out" buffer network (LINE MEMORY 5, 6 and 7) to realize work windows on a certain number (3) of scan lines of the video picture.

The block further includes digital-to-analog converters (DAC) for reconverting the luminance (Y) and chrominance (UV) processed digital streams into corresponding analog signals relative to the three components to be fed to address to the VIDEO PROCESSOR block which generates the deflection signals (RGB).

DESCRIPTION OF THE INVENTION

In an SQTV system of the conventional type, for instance as that described in Fig. 2, the invention may be implemented by modifying the architecture of the input digital data storing section.

According to an embodiment of the invention, the architecture of this section of the SQTV processing system of Fig. 2 is shown in Fig. 3.

Basically, the architecture of the invention includes, for each digital stream, a compressing and coding block (ADPCM Encoder) of data to be written in the relevant field memory, FIELD MEMORY_1 and FIELD MEMORY_2 and an ADPCM decoding and decompressing block (ADPCM Decoder) of the data read from the memory.

Conveniently, for each digital stream to be compressed according to an adaptive differential pulse code modulation scheme (ADPCM) before being written in a relevant field memory, it is useful to create suitable work windows, apportioning in practice each picture (field) into a plurality of areas in order to optimize the management of data during the various phases of compressing, coding, writing in memory, reading, decoding and decompressing.

Focusing now our attention on the FIELD MEMORY_1, and assuming to store PAL fields at a frequency of 50 Hz, to be read at a double frequency of 100 Hz, and referring to the diagram in Fig. 3 we can notice the following.

The field stored in the Y buffer of the FIELD MEMORY_1 of the diagram in Fig. 3, is made up of the sequence of 288 video lines, each one of them consisting of 720 luminance pels. These lines are used by the WINDOW GENERATOR circuit block to create a work window on which carrying out a compression. This window or picture area is compressed by the Y_ADPCM_Encoder block and then stored in the Y_FIELD MEMORY_1. At the memory output, this windows is decompressed in "raster" mode without the aid of a delay buffer of the "First-In-First-Out" type, by the Y_ADPCM_Decoder block.

Fig. 4 shows the circuit diagram of each WINDOW GENERATOR block.

By assuming for instance to be working on a window consisting of 16 pels per line and to be using 4 lines, as shown in Fig. 5, in view of the fact that the WINDOW GENERATOR is fed by video lines in the "raster" sequential mode, "First-In-First-Out" memories (LINE MEMORY) are required for delaying each pels of a video line for a time equal to the "transit" time of the whole line through the buffer. Three of these memories are required for the construction of the 4-line window.

Each line feeds the VARIANCE ESTIMATOR block with 16 pels at a time and aligned on the same vertical line. This block calculates the differences, as absolute value, among consecutive pels belonging to a window having horizontal width equal to 16 pels. Four partial sums are thus obtained at the same time. The sum of the four values is the expected

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total sum.

This solution is preferable for multiplexing the four lines pels (upstream of the VARIANCE ESTIMATOR) because multiplexing would increase the operational frequency from 13.5 Mhz to 54 Mhz, which is inconvenient to practical implementation.

These pels feed the ADPCM Encoder.

Each PAL field is thus divided into rectangular blocks having 16*4 size or more in general RxC (R lines and C columns). The maximum effectiveness of compression is obtained when R and C are selected, respectively, among integer dividers of the picture size.

The algorithm implemented by the ADPCM Encoder operates the compression of each block, that is a reduction of the number of bits required for the digital representation thereof, employing only information obtained from the block itself, in order to simplify access to the block in the compressed data stream as well as decompression of the block.

Therefore by defining an ordering of the scanning of pixels of each block, such that for each pixel, except for the first one of each line, there exists a preceding one, which can be used as predictor of the pixel itself, and by assuming that $P(i, j)$, i=1, ..., R and i=1, ..., C, is the pixel of line i and column j of a generic block, and $P'(i, j)$ is the pixel used as predictor of $P(i, j)$, the sequence of Fig. 5 is defined as follows:

* $P(i, 1)$, i=first scanned pixel of each line i=1, ..., R

* $P'(i, j) = P(i, j-1)$; i=1, ..., R and j=2, ..., C

Therefore by defining $E(i, j) = P(i, j) - P'(i, j)$ as the prediction error, it is known that the set of the prediction errors has a statistical description which can be well approximated by a sequence of random and equally distributed independent variables having a Laplacian probability density.

By exploiting this prior information of the prediction error, it is possible to compress the latter by mapping it on a small set of values $Q(k)$, k=1,...,L and L<2^B, without introducing an excessive distortion.

This mapping operation is called quantization.

By assuming that each one of the L values $Q(k)$ can be coded with a C number of bits lower than B (this being absolutely true when e.g. L=<2^C), the binary coding of each pixel submitted to the predictive process results compressed by a C/B factor.

The ADPCM compression method is applied to each one of the blocks in which the picture is divided through the following operations:

1) selection and coding in the digital stream of a suitable quantizer;
2) coding of the first pixel of each block line;
3) decorrelation, quantization and coding of all the following pixels of the block.

Selection and coding of the Quantizer

It is well known that distortion introduced by the quantization process can be reduced if all quantization values $Q(k)$ are calculated by considering the power of the signal to be quantized. It is also known that different portions of a digital picture may show very different power values. The present method defines the set of $Q(k)$ values relevant to each block depending on the power of the block itself, as follows:

* the set of $Q1(k)$ k=1,...,L values used in case of unit power, is known both to the encoder and to the decoder;
* the power U of the block is estimated and coded in the digital stream;
* $Q(k)$ values actually used for the block are calculated as:

$$Q(k) = Q1(k) * U; k=1,...,L$$

The evaluation of the block power can be simply made in the Laplacian statistical hypothesis of the prediction error. In fact, in this case the power can be calculated by multiplying the mean of absolute values of the block prediction errors by the square root of two. Power coding can be made simply by scaling about the maximum value and by representing the result on a number of bits K, thus essentially realizing an even quantization.

In selecting the prediction error quantizer the peak value of the quantization error must be taken into account too, because in the case of large prediction errors it could happen that the maximum value rendered by the quantizer, according to the diagram shown below, be too small. Therefore, simultaneously to the variance calculation, also the peak values of the prediction error are calculated for each group G of horizontal consecutive lines (e.g. G=2). One bit for each one of these groups of pixel is added to the coding, in order to signal the occurrence of an excessive peak of the prediction error and, consequently a quantizer corresponding to a 2*U power in case of a pair of lines is selected.

Coding of the first pixel of each line of the block

The first pixel of the block, indicated above as P(i,1) is not subject to any prediction and therefore it is coded according to its original resolution by a number B of bits.

Compared to the known technique, the scanning path of the window is modified. This permits to adapt the decompression to the need of obtaining the raster format at output of the FIELD MEMORY.

Decorrelation, quantization and coding of all the other pixels of the block

For each pixel P of the block, the pixel P' is adopted as predictor according to what was defined above. It must be noticed that this predictor, following the scanning order shown, has already been quantized and reconstructed, and therefore is not obtained from the original picture; this permits an enhanced quality control of the picture, consistently with the ADPCM technique.

Example of compression at N bits per pixel:

With reference to the scanning example shown in Fig. 5, a block R*C of pixels after the WINDOW GENERATOR block is taken in consideration.

The total bits employed for the block compression are equal to:

$$K + (8*R) + (R*C-1) * N + R/G$$

where:

K = bits employed for power coding.
8 = bits employed for the first pixel in the scanning of each line.
N = bits employed for quantization
(R*C-1) * N = bits employed for DPCM coding of the remaining pixels
R/G = bits to signal the altered quantizer in the R/G groups of lines

In the case: K=6, R=4, C=16, N=4, G=2 the following total is obtained:

$$6 + 8*4 + (4*16-1) * 4+4/2 = 280 \text{ bits/block}$$

In the case: K=6, R=4, C=16, N=3, G=2 the following total is obtained:

$$6 + 8*4 + (4*16-1) * 3+4/2 = 220 \text{ bits/block}$$

versus 4*16*8 = 512 bits requested by the original representation.

Example of compression of a PAL 4:2:2 field

Each field consists of 3,240, 4*16 luminance blocks and of 1,620, 4*16 blocks for each chrominance component; each luminance and chrominance block is coded with a number of bits equal to (4*16*8) =512 bits.

Each field, broken down in blocks, occupies the following number of bits:

- Y component [(720*288) / (4*16)] * 512 =	1,658,880 bits
- U component [(360*288) / (4*16)] * 512 =	829,400 bits
- V component [(360*288) / (4*16)] * 512 =	829,400 bits
Total :	3,317,760 bits

On the contrary, considering for instance a 4 bit/pixel compression of luminance and a 3 bit/pixel of chrominance, we would obtain:

- Y component [(720*288) / (4*16)] * 280 =	907,200 bits
- U component [(360*288) / (4*16)] * 220 =	356,400 bits
- V component [(360*288) / (4*16)] * 220 =	356,400 bits
Total :	1,620,000 bits

the compression factor obtained is equal to 2,048, thus enabling a 50% compression of each field.

Example of decompression of a PAL 4:2:2 field

During the decompression phase, the raster format must be generated. Referring to the example in Figures 5 and 6, assuming to be decompressing all the pels belonging to line 3 and next to start decompression of those of the m and (m+1)th block of the luminance component, the following bits must be read from the m-th block:

K = 6   bits employed for power coding
8 =   bits employed for the first pixel of the portion of line 3
C-1*N=60   bits employed for DPCM coding of remaining pixels of line 3
1   bit to signal that the quantizer is altered.

In this way the ADPCM Decoder block of the diagram of Fig. 3 shall have all the information required and sufficient to decompress all the 16 pel groups of each 4*16 block and belonging to the video line being subjected to the following processing.

Example of application to a SQTV decoder

Considering the relations shown, it is possible to define the architecture for a global memory requisite reduced to 3.1 Mbits if a 50% compression of FIELD MEMORIES is assumed.
This result is reached by recompressing the fields stored upstream the NOISE REDUCTION block, according to the diagram shown in Fig. 3.
The compression is suited to the block 4*16 produced by the WINDOW GENERATOR, according to the adaptive DPCM scheme. In particular for luminance blocks 4*16 a 4 bits compression has been selected, while for chrominance 4*16 blocks, a 3 bits compression has been selected.
Therefore the memory requisite of the 2 FIELD MEMORIES is:

$$1,620,000 * 2 = 3,240,000 \text{ bits}$$

Considering the objective of integrating the FIELD MEMORIES in the SQTV chip without resorting to external memory devices, the above stated result enables a large saving of silicon area required for their realization.
Fig. 7 shows a functional diagram of each ADPCM Encoder block.
Referring to Fig. 7, the ADPCM Encoder block includes a 64*8 bit buffer (BLOCK BUFFER) for the acquisition of input data. A dedicated circuit (VARIANCE ESTIMATOR) calculates the average value of pels of each input data block and the mean of the sum of absolute values of differences between each pel of the data block. With these parameters it is possible to evaluate the input data (pels) block variance. The estimated value of the variance is used as a conditioning coefficient pointer of the quantizer (QUANTIZER) which can be pre-set and be permanently recorded in a dedicated read only memory (ROM). As an alternative, a less expensive solution may be the utilization of a pre-settable combinatory logic (PLA) circuitry, in order to produce one or more pre-set digital values according to the variance datum applied at the input.
The DPCM compression network, suitable to generate a predictor value to apply to the relevant input of the differentiating stage (-), consists of a two-input multiplexer (MUX), at a first input of which the value of the first pel (A1) of each input data block is applied, while the predictor value produced by the network is applied to the other input. The adder stage (+) receives through a first input the output stream of the quantizer circuit (QUANTIZER) to be added to the output value of the multiplexer (MUX). The sum datum produced by the adder stage (+) is applied to the input of a limiter circuit (LIM. 0-255) whose output stream is fed to the input of a predictor value generator circuit (COEFF).
The limiter stage (LIM. 0-255) can be made of a dedicated combinatory logic circuit. The utilization of this stage becomes necessary to compensate possible straying of the maximum value of a pixel from the limit assigned, which in the case of a 8-bit coding of a pixel value, is fixed at 255. In fact, during the compression and decompression phases,

the pixel value could randomly exceed the limit value of 255 and in this case the limiter circuit confines the maximum value of the pixel within the allowed limit.

A coding stage (CODER) for writing compressed data into the field memories, at three bits for chrominance data and four bits for luminance data, receives at input the output stream of the quantizer circuit (QUANTIZER) and writes data so recompressed in the relevant buffers of the field memory.

Fig. 8 shows a functional diagram of each ADPCM DECODER block.

Assuming to read from the memory an ADPCM compressed 4*16 block of luminance data, from these a variance value is obtained which is fed to the ROM (or to the PLA) to point one of the values stored therein. The T0, T1, T2, T3, T4, T5, T6 and T7 values feeding the multiplexer MUX are thus produced. In case of luminance data decompression, the 4-bit subwords that are obtained from the data block drive the selection of the T values by the MUX.

Finally, the current T value, besides becoming the decompressed pel, becomes also the value to be added to the next value selected by the MUX.

This process is initialized by the first pel of the block which is not subject to compression and decompression.

Of course, the actual embodiments of the various functional blocks of the ADPCM ENCODER and of ADPCM DECODER diagrams of Figures 7 and 8, may be different. Practical embodiments of these functional blocks are described in the specification and drawings of the application for European Patent No. 96830106.9, filed on March 11 1996, in the name of the same Applicant, whose content is herein included by express reference.

Figures 9, 10 and 11 show a detailed functional diagram of the VARIANCE ESTIMATOR block of Fig. 7, according to a preferred embodiment. Common functional symbols are employed in the figures and therefore they may be immediately read and understood for a technician with ordinary skills in the art and a reiterated definition and description of each stage forming the VARIANCE ESTIMATOR circuit is not deemed necessary for a complete understanding of the architecture or for its practical implementation.

Claims

1. SQTV processor for converting a video signal received at an interlaced scanning frequency of 50 or 60 Hz, respectively to an interlaced scanning frequency of 100 or 120 Hz and implementing algorithms of noise filtering and of edge definition, including an analog-digital converter (ADC) of analog input signals of luminance and chrominance, at least a field memory (FIELD MEMORY_1) where digital blocks of luminance (Y) value and blocks of values of each one of the two chrominance (U, V) components of said converted video signals are stored, one "First-In-First-Out" (LINE MEMORY) register for digital values read from said filed memory containing the pixels of a whole line of each field, a noise filtering block (NOISE REDUCTION), a sampling frequency converter (SRC) of said fields from 50 or 60 Hz to 100 or 120 Hz, means of conversion of the vertical format (VFC), means of edge definition (PE) enhancement and means of digital-to-analog conversion (DAC) of the processed luminance and chrominance (YUV) signals,
   characterized in that it comprises

   means for compressing and coding said converted video signals according to an adaptive differential pulse code modulation (ADPCM) scheme of said digital values to be stored in said field memory (FIELD MEMORY_1);
   means of ADPCM decoding and decompressing of data read from said field memory (FIELD MEMORY_1).

2. The SQTV processor according to claim 1, characterized in that it comprises

   a second field memory (FIELD MEMORY_2) employed as field delay for field interpolation functions for filtering pulse and gaussian noise by means of said noise filtering block (NOISE REDUCTION);
   compressing and coding means (ADPCM Encoder) of said converted video signals according to an adaptive differential pulse code modulation compression scheme of said digital signals to store them in said second field memory (FIELD MEMORY_2);
   ADPCM means of decoding and decompressing (Decoder) of data read from said second field memory (FIELD MEMORY_2).

3. The SQTV processor according to claim 2, characterized in that said field memories (FIELD MEMORY_1 FIELD MEMORY_2) are defined in external DRAM device.

4. The SQTV processor according to claim 1 or 2, characterized in that said field memory or memories (FIELD MEMORY_1, FIELD MEMORY_2) are integrated on the same chip of the processor.
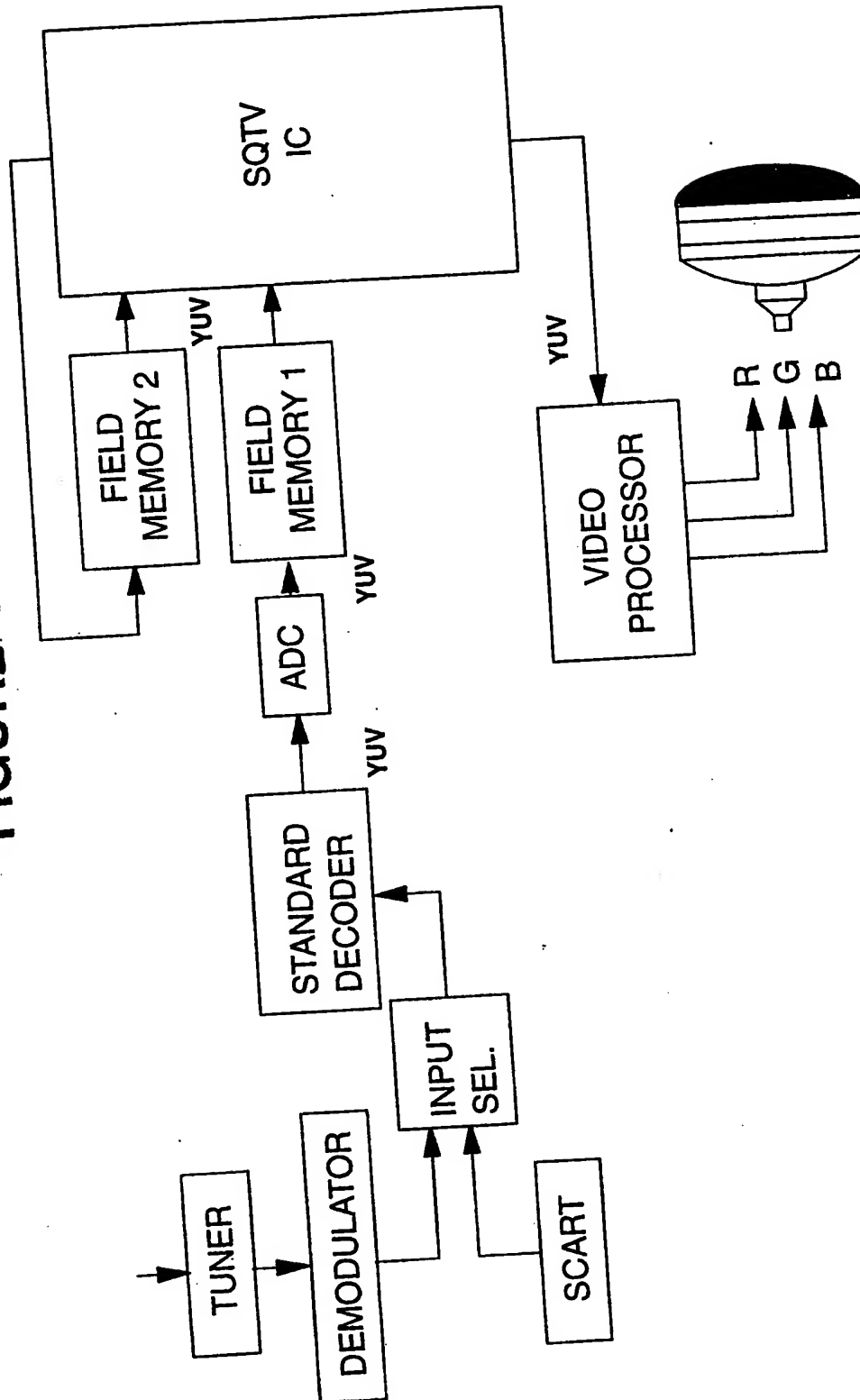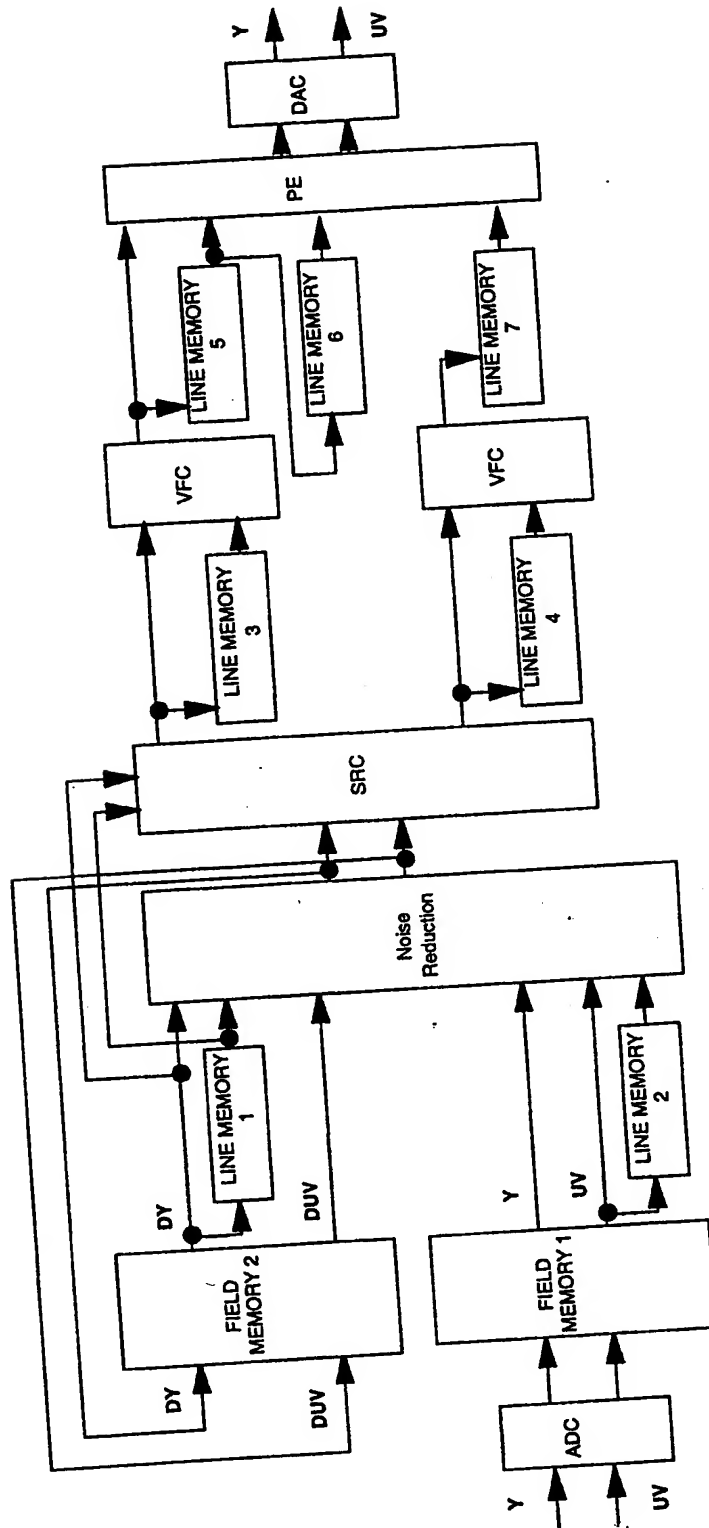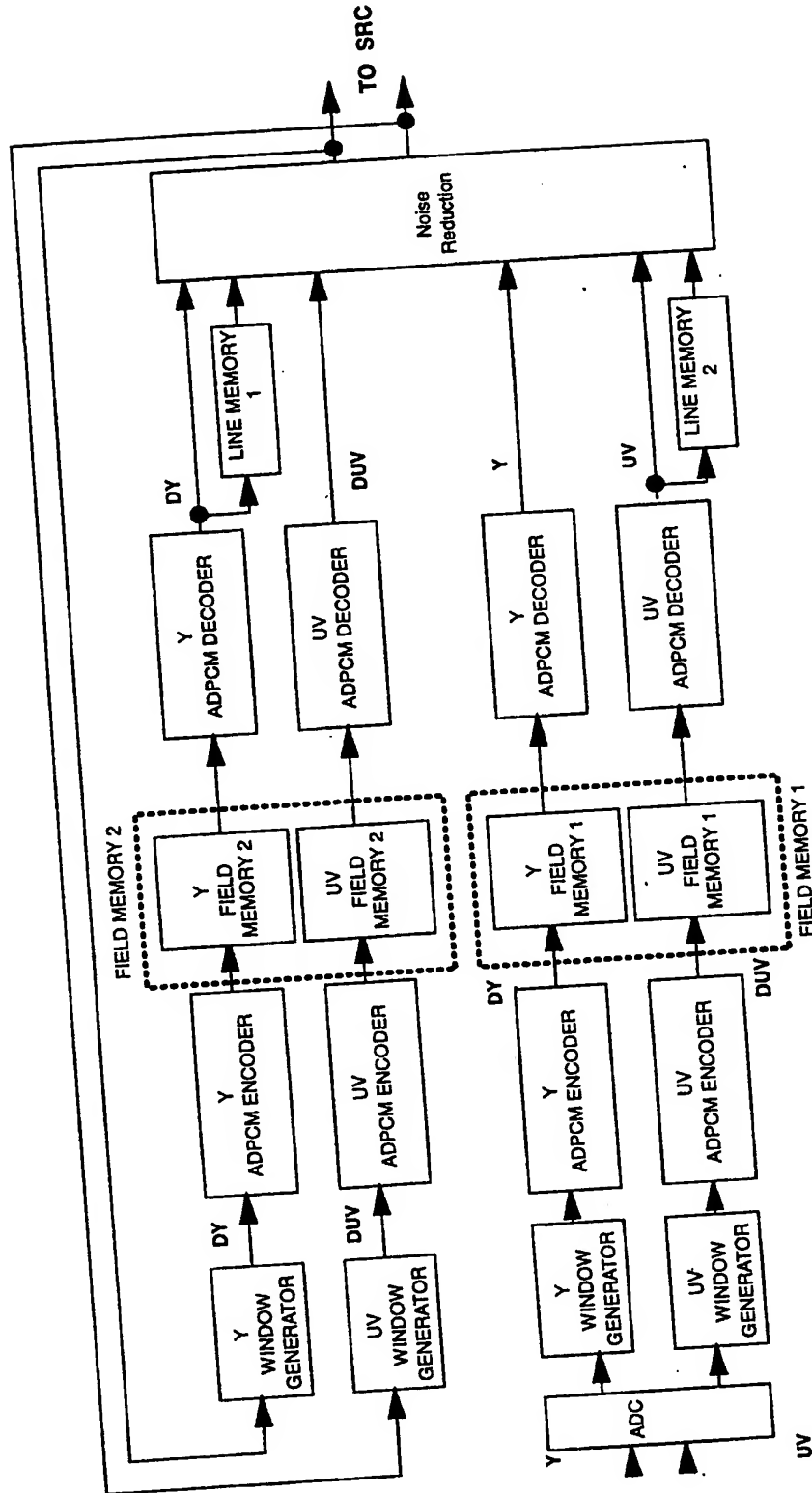
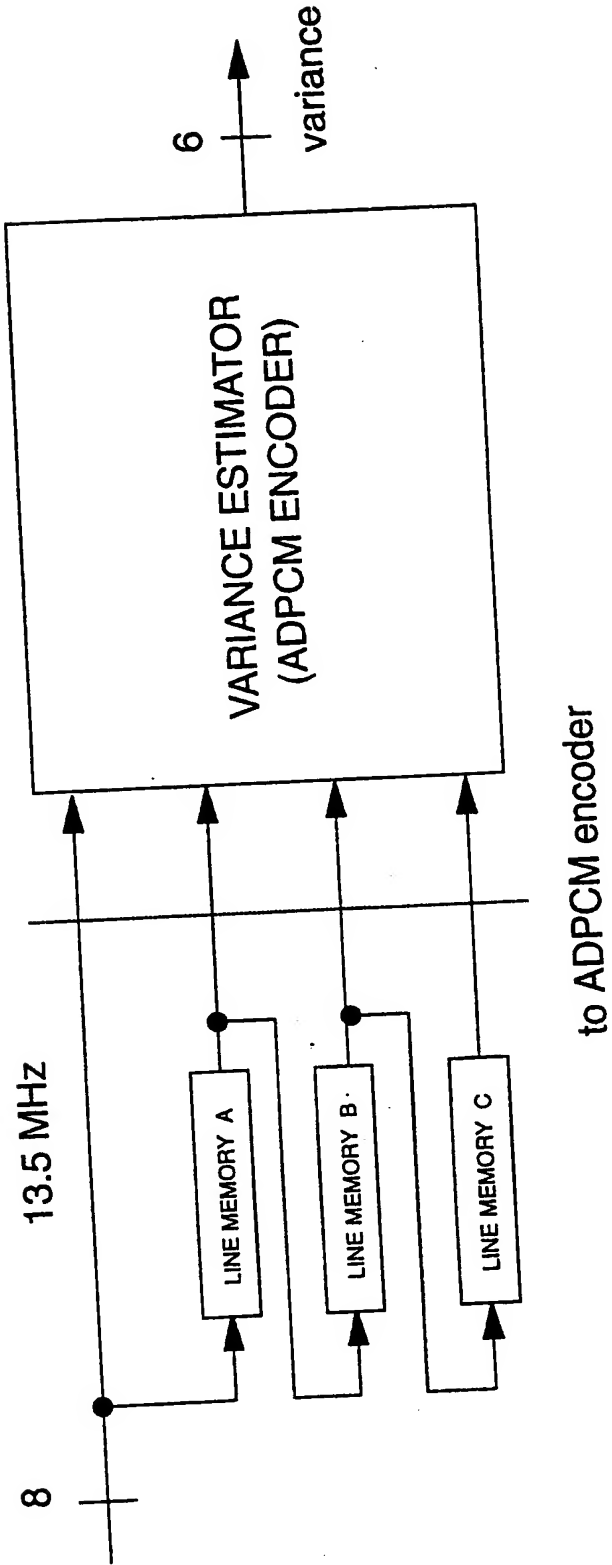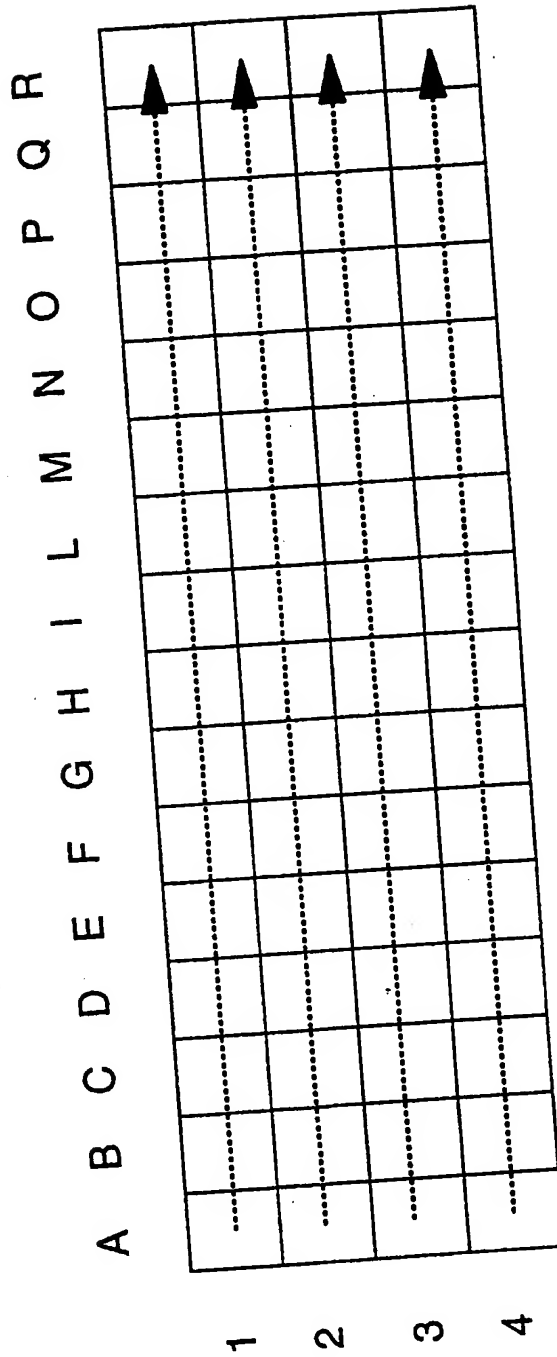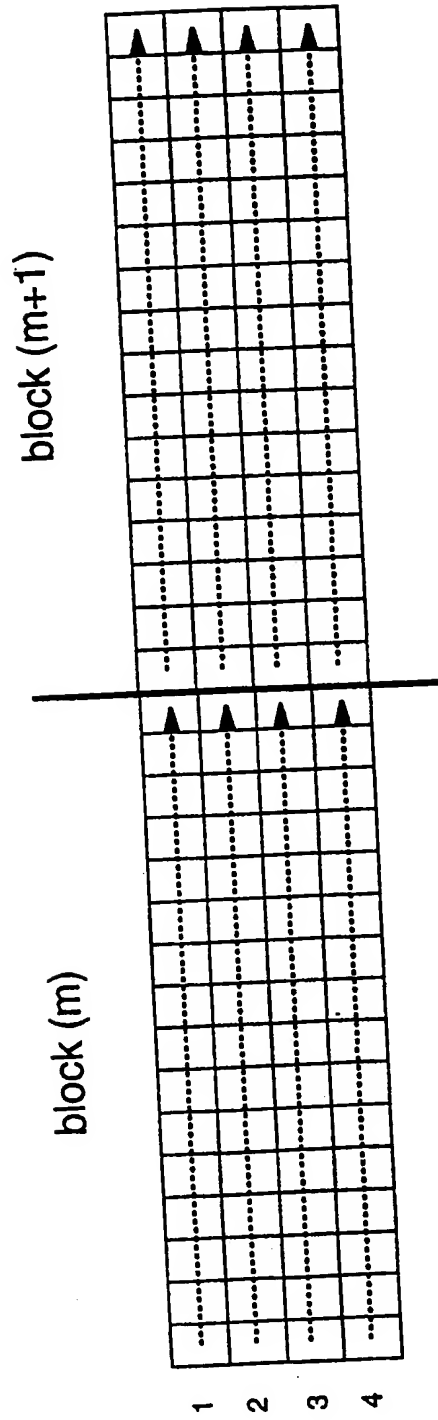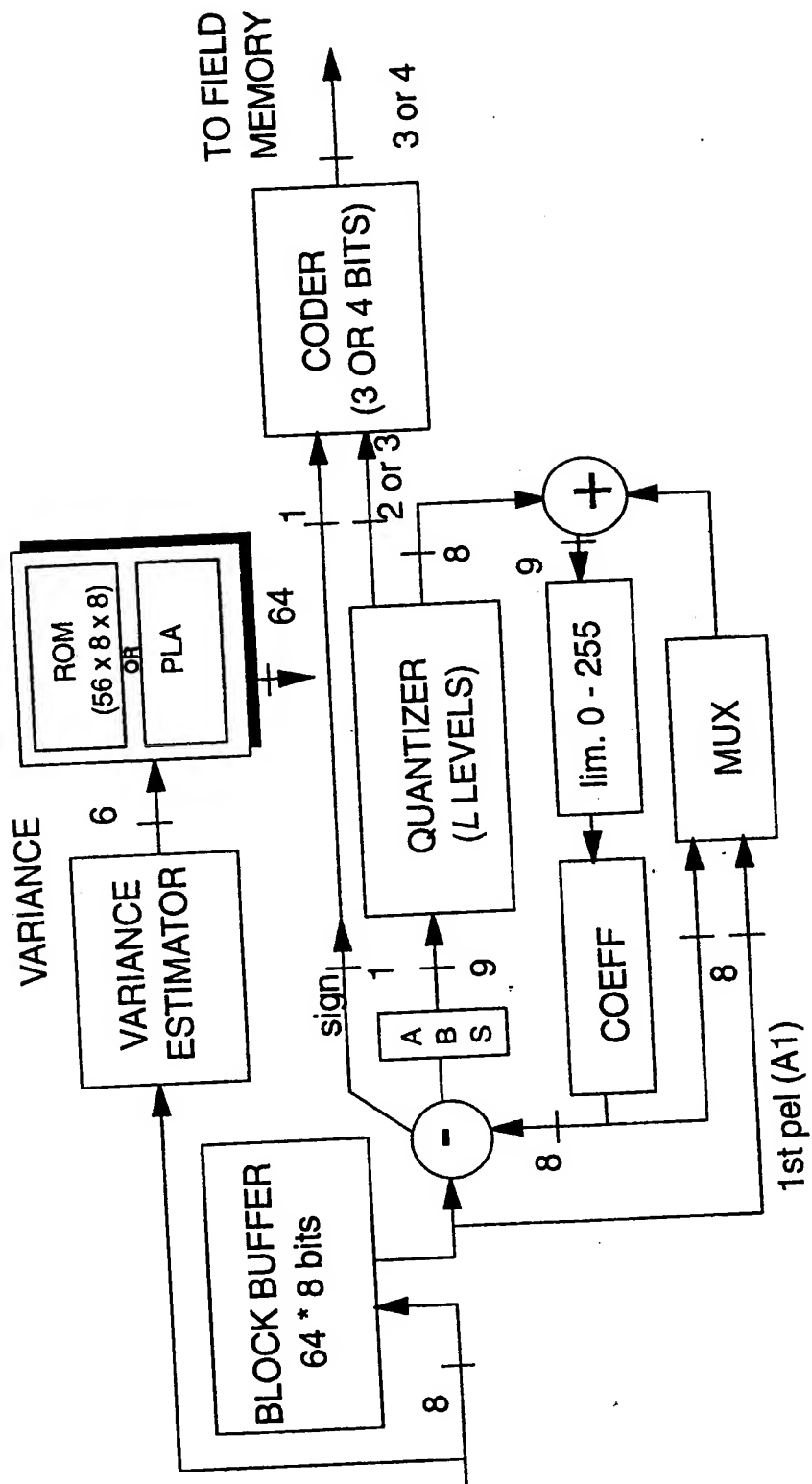# FIGURE 1

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

FIGURE 6

block (m+1)

block (m)

1
2
3
4

FIGURE 7

FIGURE 8

DECOMPRESSED PELS
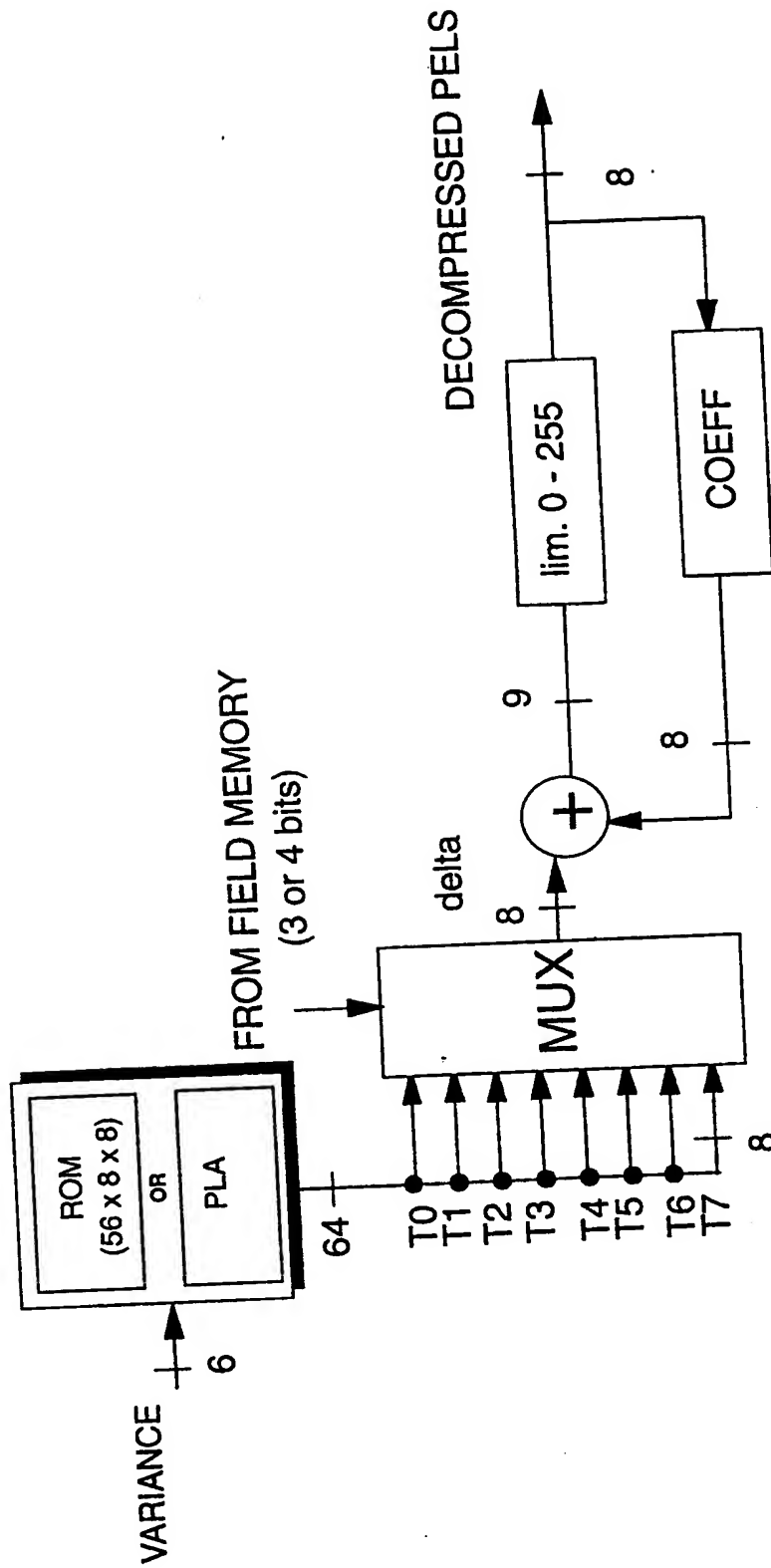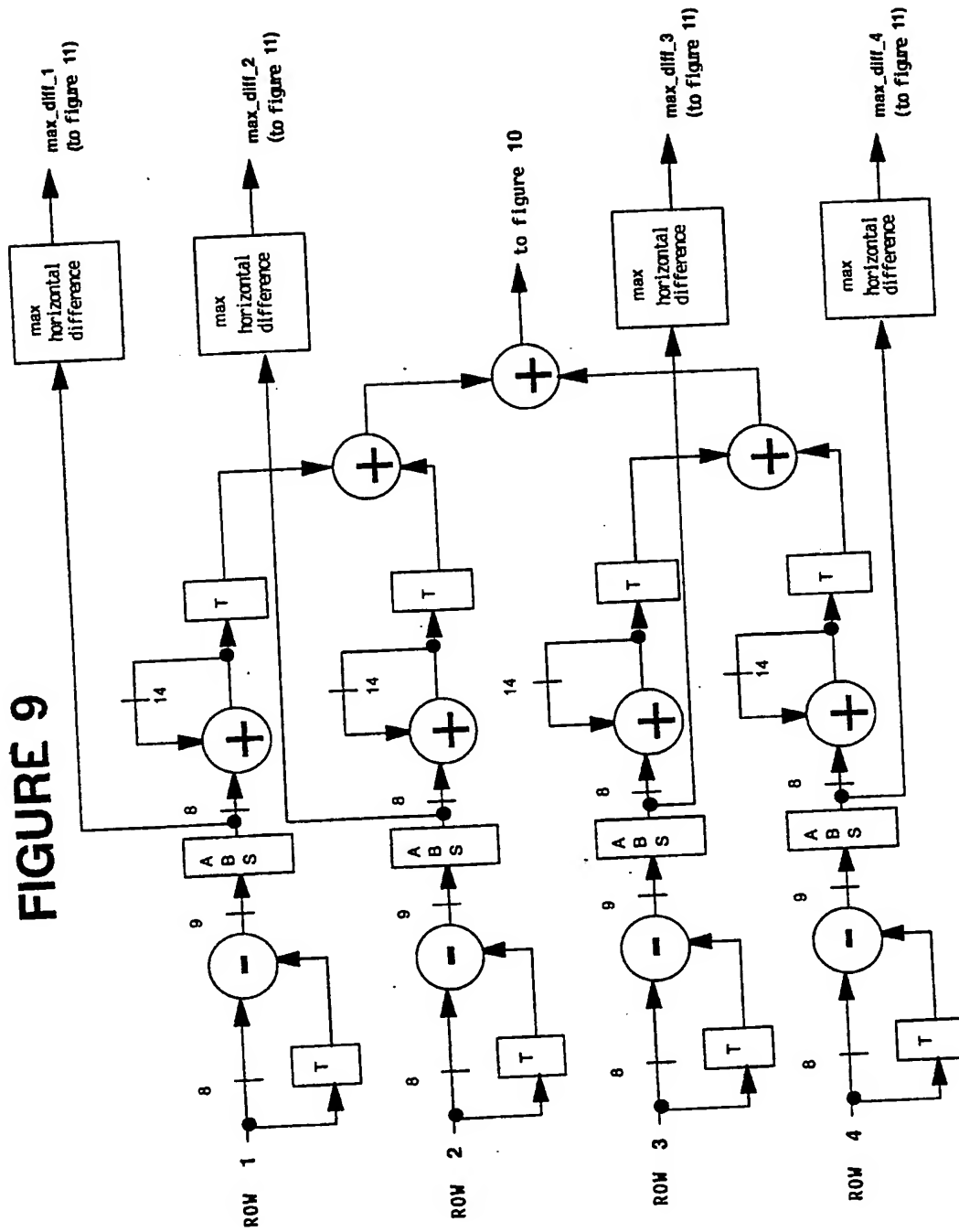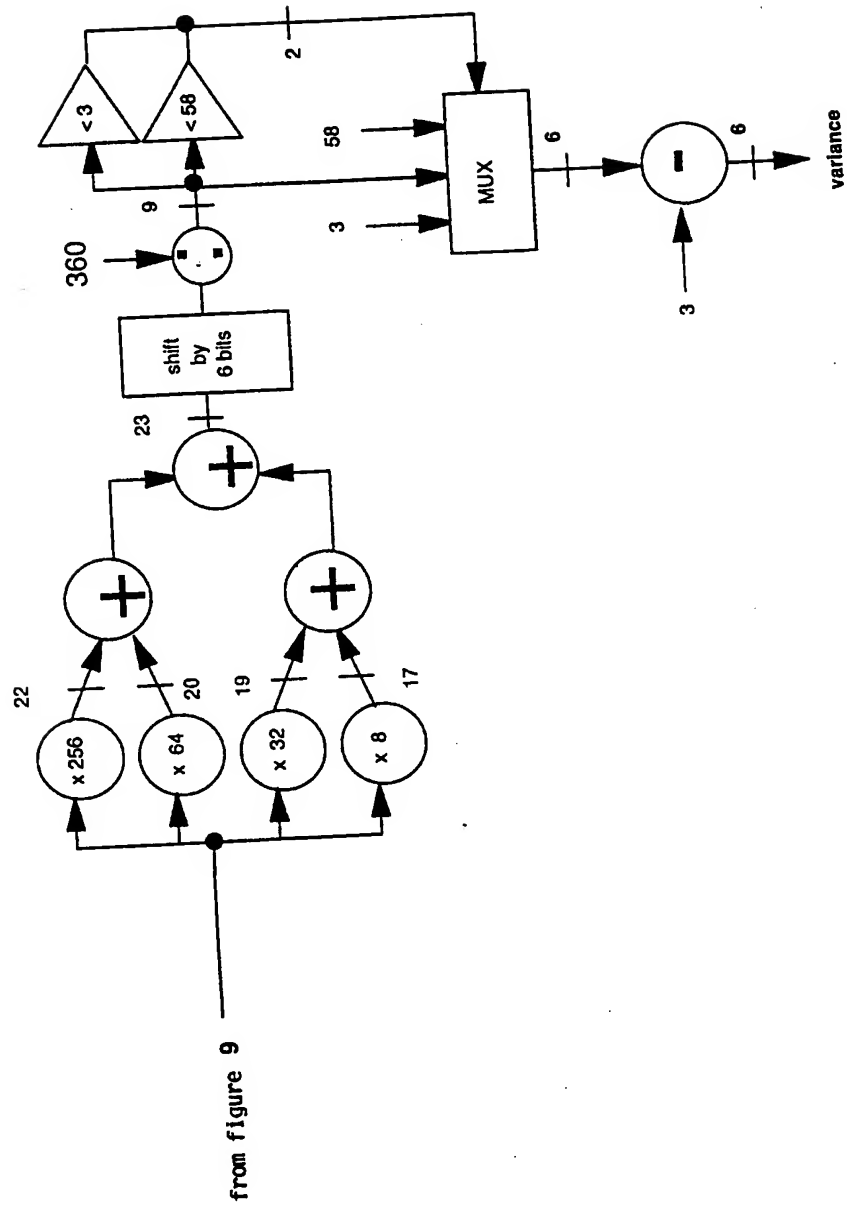
FIGURE 9

FIGURE 10

FIGURE 11
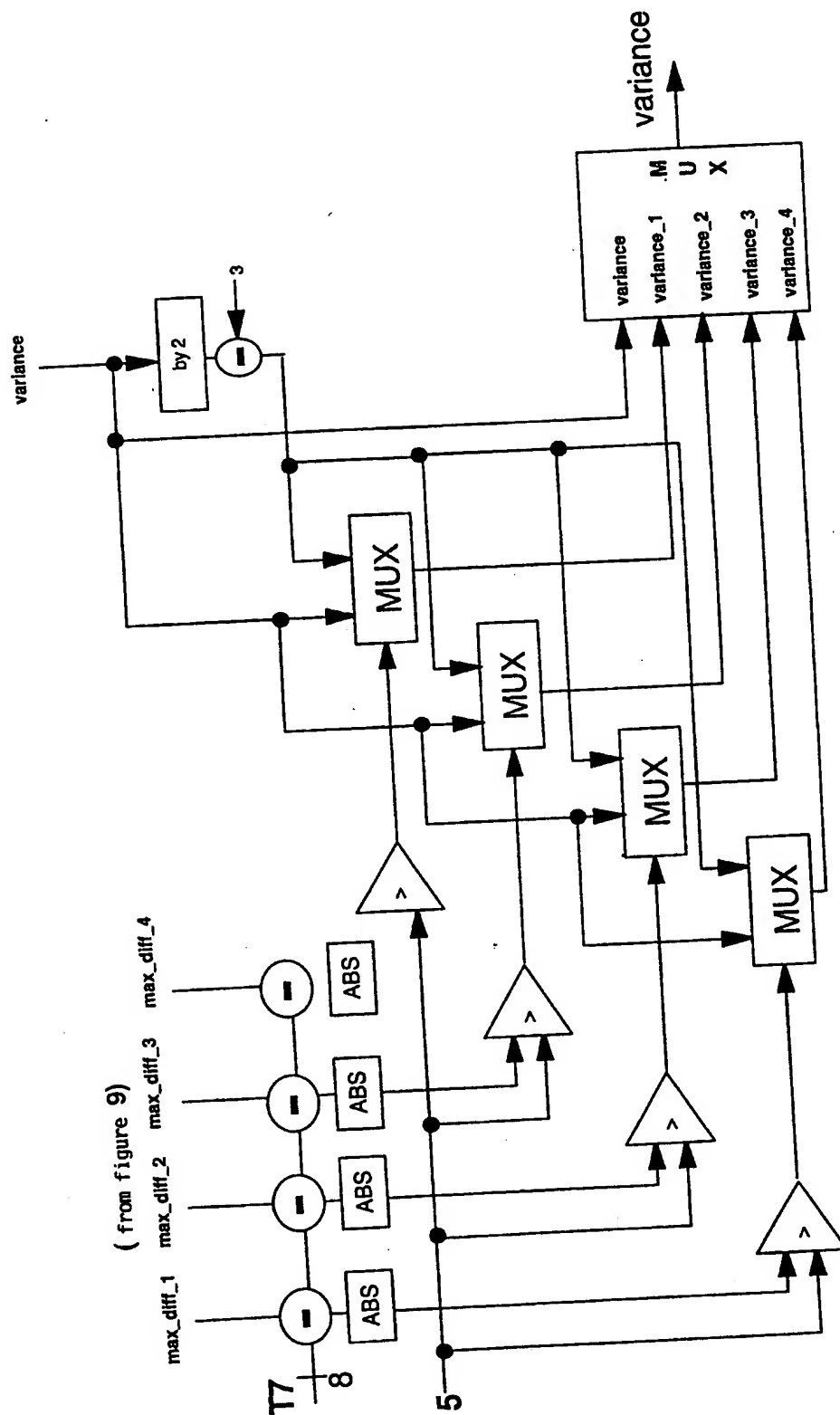
EUROPEAN SEARCH REPORT

Application Number

EP 96 83 0134

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PROCEEDINGS OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE, SAN DIEGO, MAY 1 - 4, 1994, no. CONF. 16, 1 May 1994, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 111-114, XP000492867 D'ALTO V ET AL: "MULTIPURPOSE SCANNING RATE CONVERTER IC FOR IMPROVED QUALITY TELEVISION" * page 111, column 1, line 15 - page 113, column 2, line 10 * ---	1-4	H04N5/44
A	PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS (ICCE), ROSEMONT, ILL., JUNE 6 - 8, 1990, no. CONF. 9, 6 June 1990, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 324-325, XP000169927 HIROSHI MIYAGUCHI ET AL: "DIGITAL TV WITH SERIAL VIDEO PROCESSOR" * page 324 - page 325 * ---	1-4	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	EP-A-0 624 032 (GOLDSTAR CO.LTD.) * column 4, line 20 - column 6, line 55 * -----	1-4	H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	31 July 1996	Materne, A